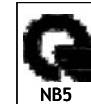
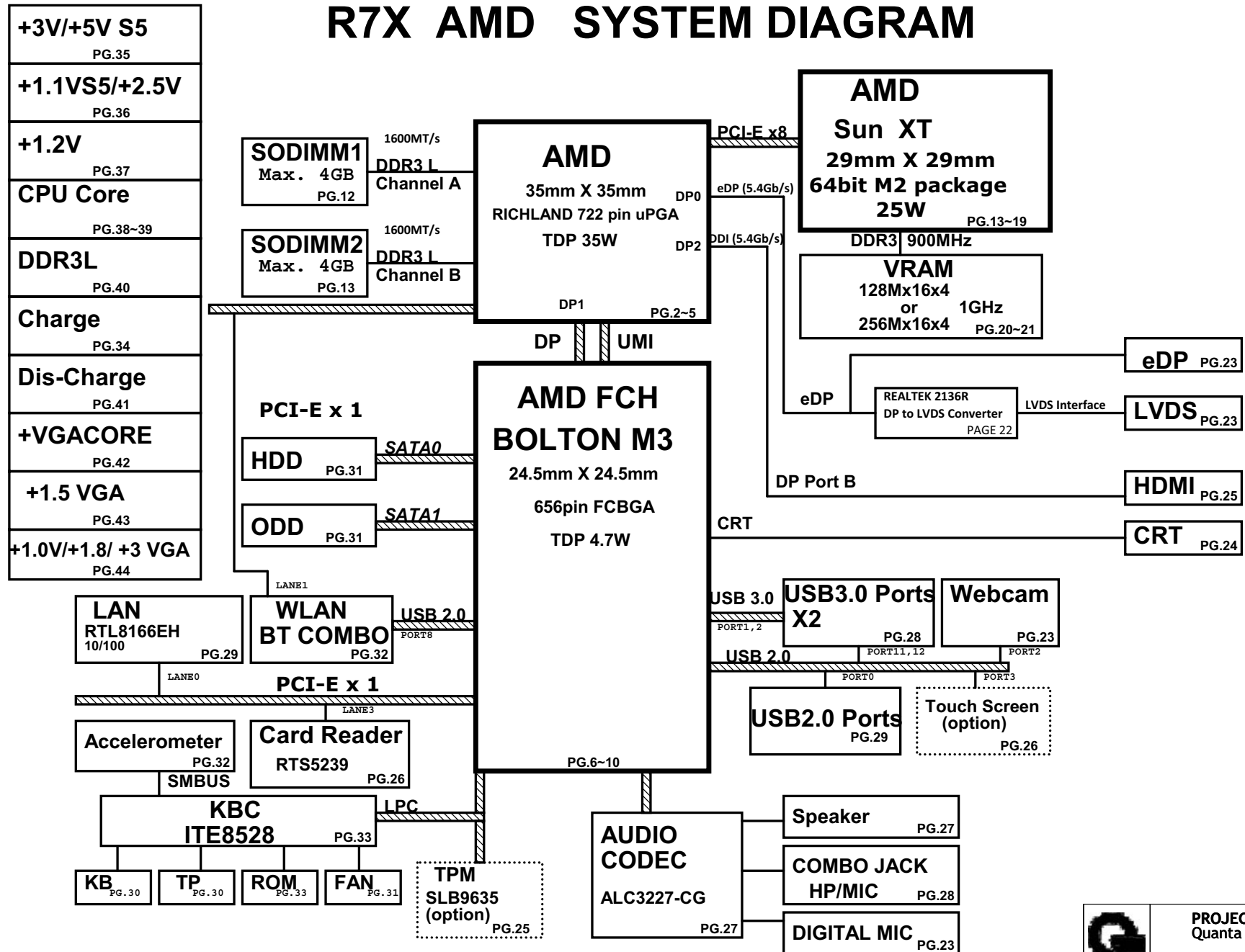


R7X AMD SYSTEM DIAGRAM



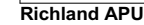
PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number BLOCK DIAGRAM	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 1 of 43	



HDT CONN
88511-2001-20p-l

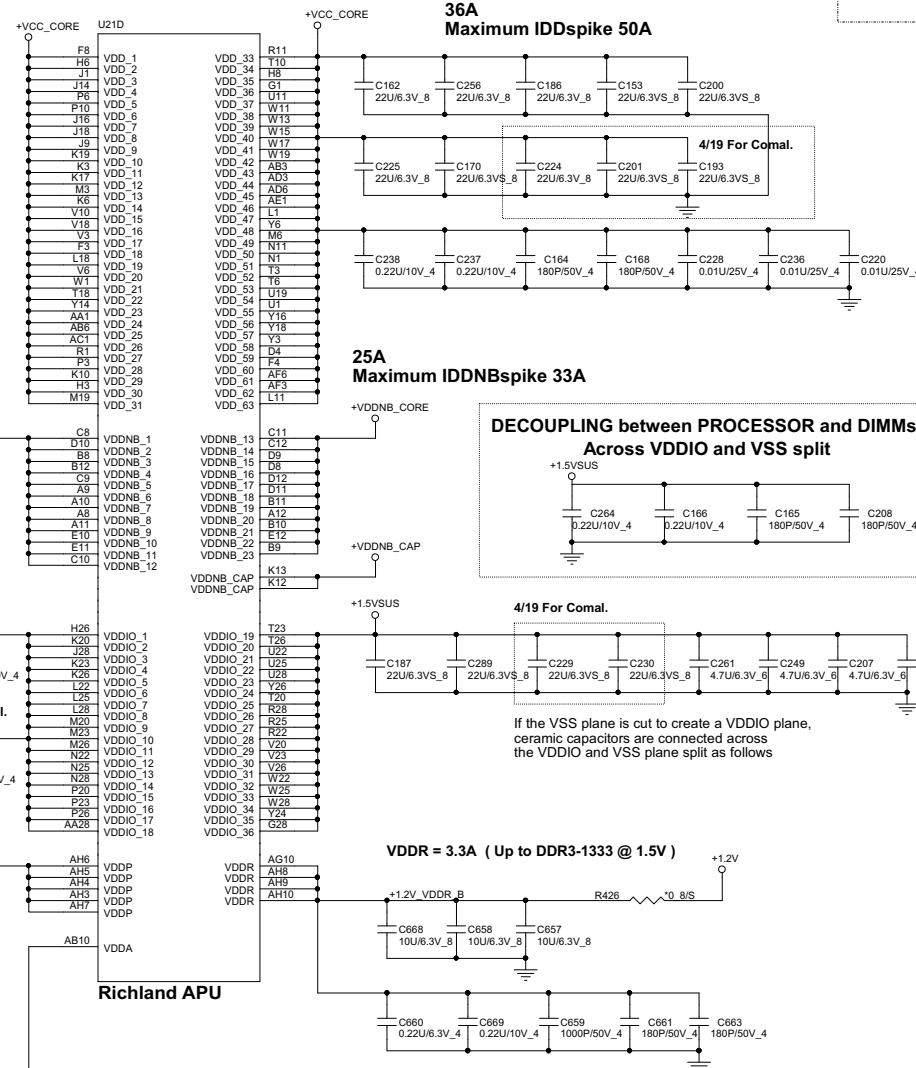
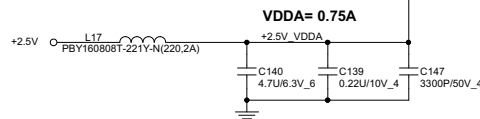
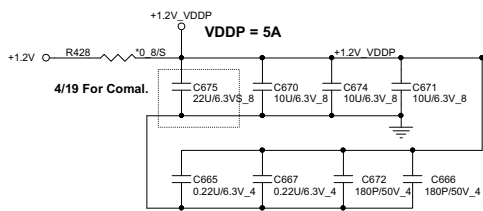
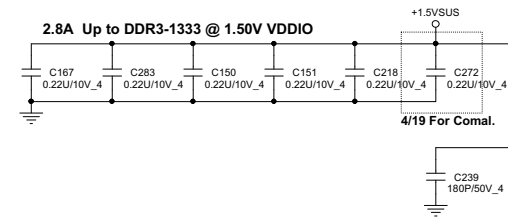
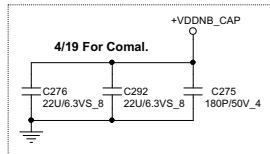
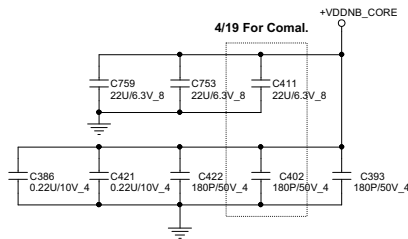
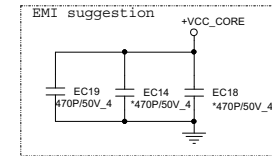
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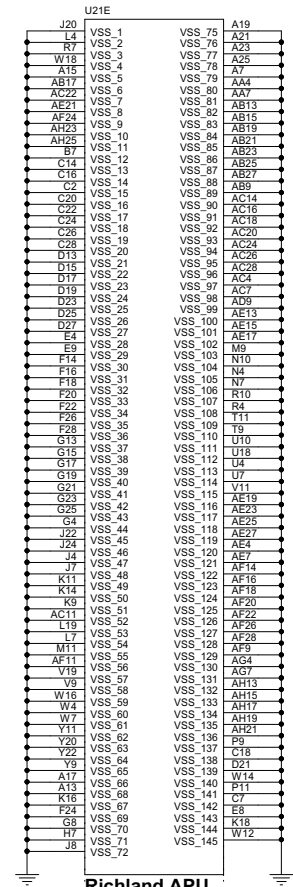


APU POWER TABLE

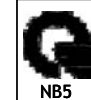
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



Richland APU

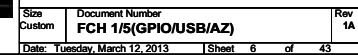


Richland APU



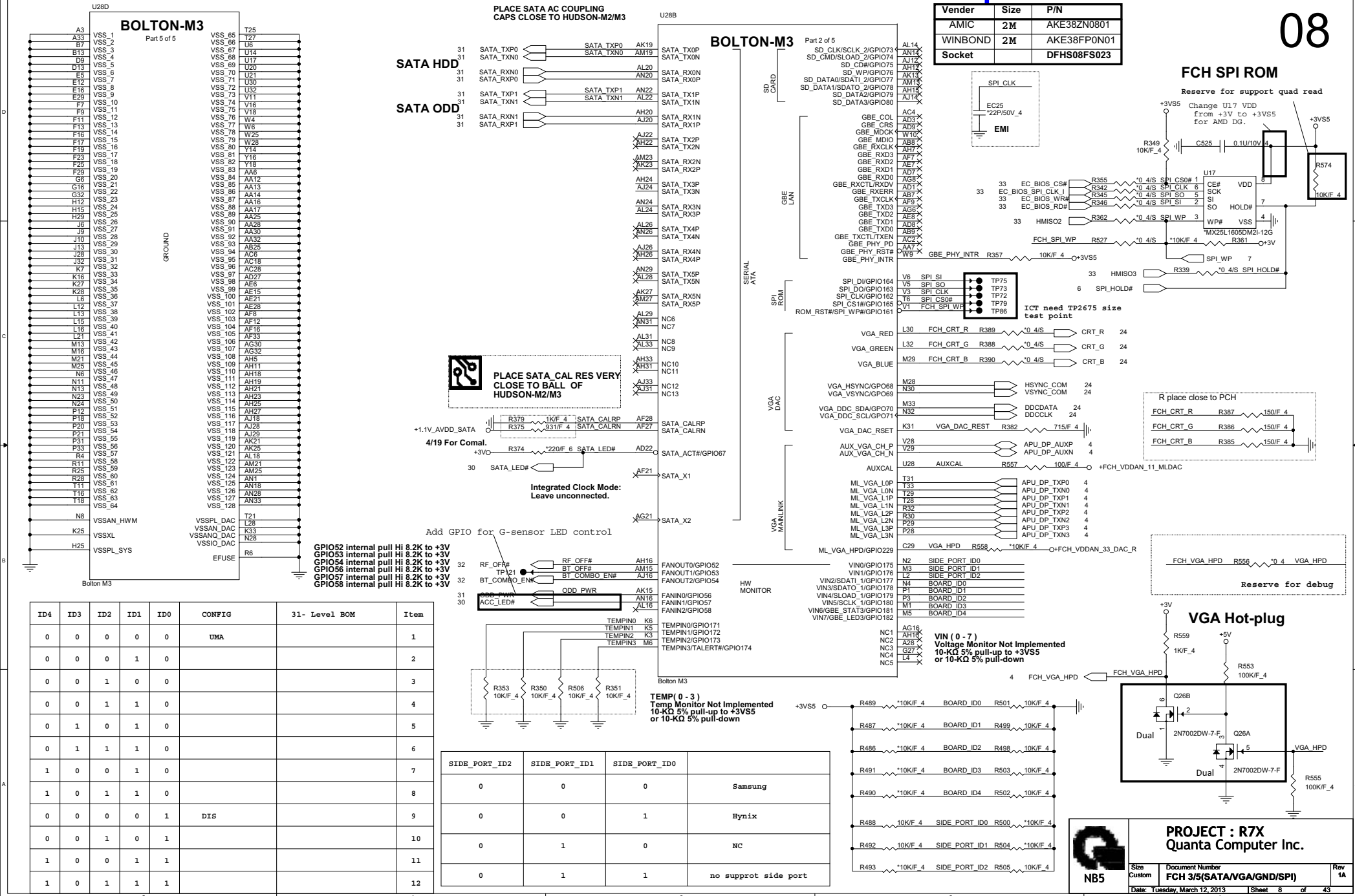
PROJECT : R7X
Quanta Computer Inc.

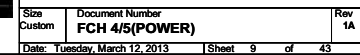
Size Custom	Document Number APU 4/4(Power/GND)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 5 of 43	





Size Custom	Document Number FCH 2/5(ACPI/PCI/CLK)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 7 of 43	

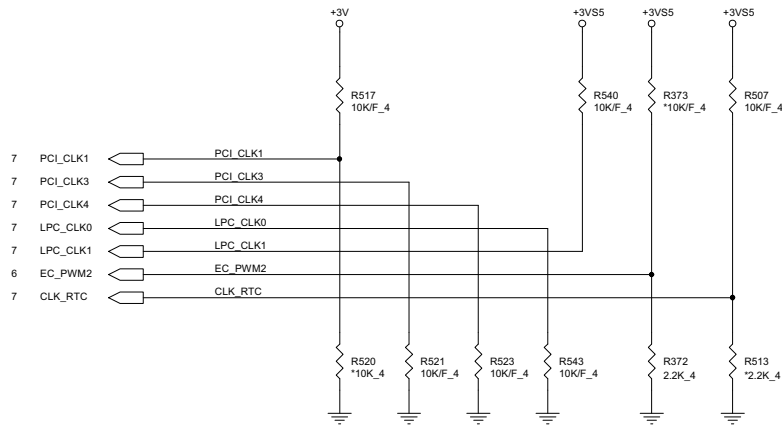




STRAPS PINS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

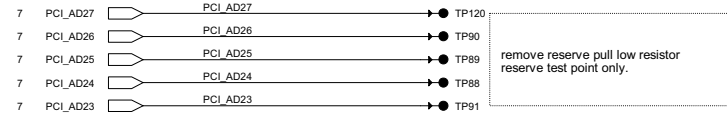


REQUIRED STRAPS

		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	*****	ALLOW PCIe Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM S5 PLUS MODE ENABLED

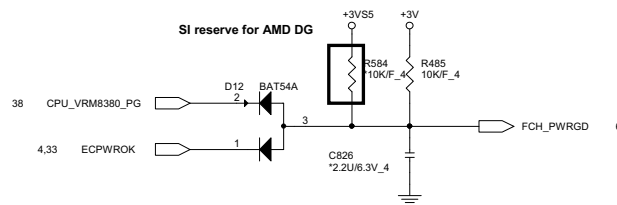
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

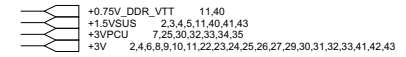
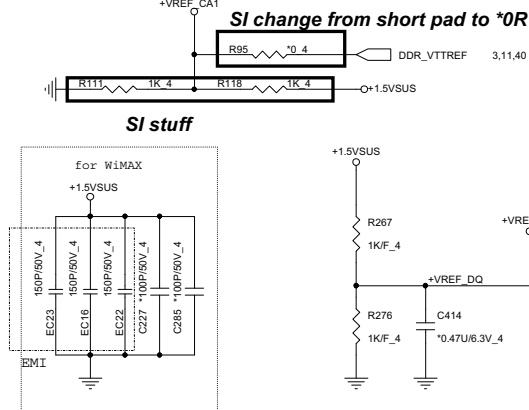
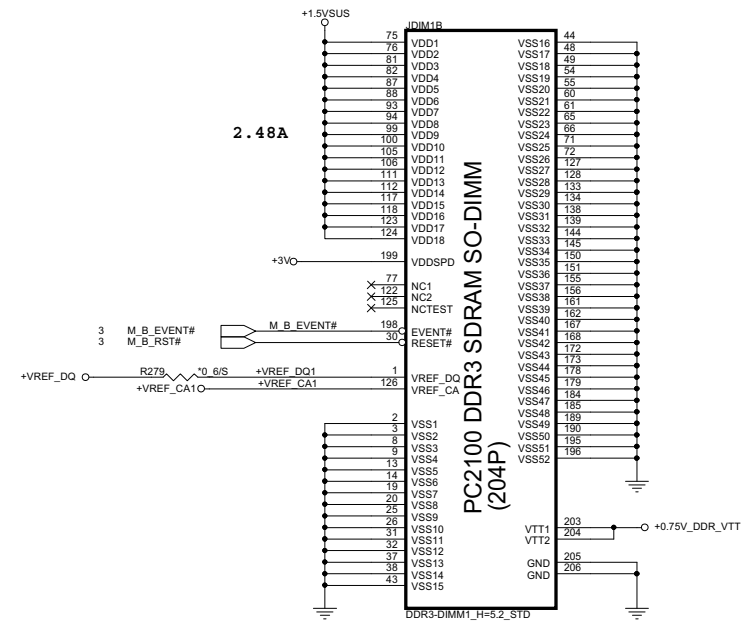
FCH_PWRGD



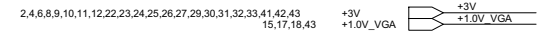
PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number FCH 5/5(Strap &PWRGD)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 10 of 43	





Size Custom	Document Number DDR3 DIMM1-STD (5.2H)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 12 of 43	



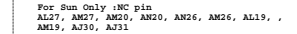
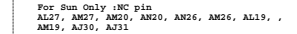
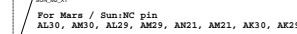
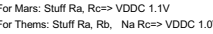
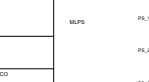
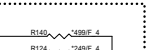
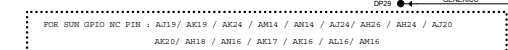
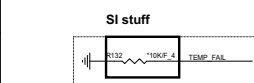
Size Custom	Document Number SUN_PCIE_Interface	Rev 1A
Date: Tuesday, March 12, 2013		Sheet 13 of 43

For Mars / Sun : DP A to D Port: all NC pin

```

: For Sun only :
: AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin
:

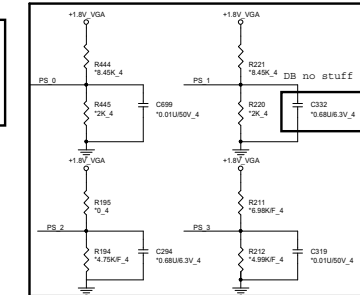
```



$R_{in} = (Ohm)$	$R_{out} (Ohm)$	$PR = (2.2 \pm)$
100	100	0.500
100	200	0.333
100	300	0.250
100	400	0.200
100	500	0.167
100	600	0.143
100	700	0.125
100	800	0.111
100	900	0.100
100	1000	0.091
100	1500	0.067
100	2000	0.050
100	3000	0.033
100	4000	0.025
100	5000	0.020
100	6000	0.017
100	7000	0.014
100	8000	0.012
100	9000	0.011
100	10000	0.010
100	15000	0.007
100	20000	0.005
100	30000	0.003
100	40000	0.002
100	50000	0.002
100	60000	0.001
100	70000	0.001
100	80000	0.001
100	90000	0.001
100	100000	0.001
100	150000	0.000
100	200000	0.000
100	300000	0.000
100	400000	0.000
100	500000	0.000
100	600000	0.000
100	700000	0.000
100	800000	0.000
100	900000	0.000
100	1000000	0.000
100	1500000	0.000
100	2000000	0.000
100	3000000	0.000
100	4000000	0.000
100	5000000	0.000
100	6000000	0.000
100	7000000	0.000
100	8000000	0.000
100	9000000	0.000
100	10000000	0.000
100	15000000	0.000
100	20000000	0.000
100	30000000	0.000
100	40000000	0.000
100	50000000	0.000
100	60000000	0.000
100	70000000	0.000
100	80000000	0.000
100	90000000	0.000
100	100000000	0.000
100	150000000	0.000
100	200000000	0.000
100	300000000	0.000
100	400000000	0.000
100	500000000	0.000
100	600000000	0.000
100	700000000	0.000
100	800000000	0.000
100	900000000	0.000
100	1000000000	0.000
100	1500000000	0.000
100	2000000000	0.000
100	3000000000	0.000
100	4000000000	0.000
100	5000000000	0.000
100	6000000000	0.000
100	7000000000	0.000
100	8000000000	0.000
100	9000000000	0.000
100	10000000000	0.000
100	15000000000	0.000
100	20000000000	0.000
100	30000000000	0.000
100	40000000000	0.000
100	50000000000	0.000
100	60000000000	0.000
100	70000000000	0.000
100	80000000000	0.000
100	90000000000	0.000
100	100000000000	0.000
100	150000000000	0.000
100	200000000000	0.000
100	300000000000	0.000
100	400000000000	0.000
100	500000000000	0.000
100	600000000000	0.000
100	700000000000	0.000
100	800000000000	0.000
100	900000000000	0.000
100	1000000000000	0.000
100	1500000000000	0.000
100	2000000000000	0.000
100	3000000000000	0.000
100	4000000000000	0.000
100	5000000000000	0.000
100	6000000000000	0.000
100	7000000000000	0.000
100	8000000000000	0.000
100	9000000000000	0.000
100	10000000000000	0.000
100	15000000000000	0.000

$R_{\text{p,d}}$ (nm)	$R_{\text{p,d}}$ (nm)	$\text{loss}_{\text{S,d}}(\%)$
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

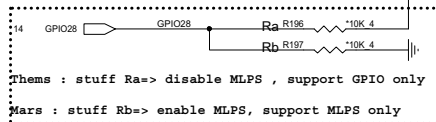
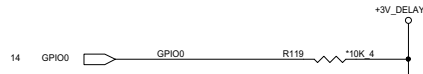
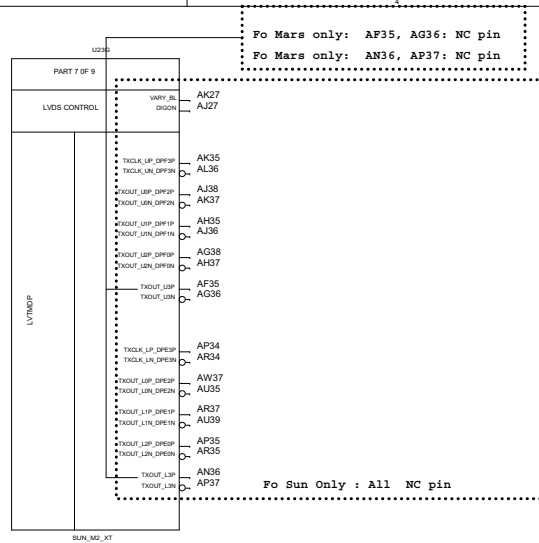
BIT5 => BIT1	
PS0	=> 11001
PS1	=> 11001
PS2	=> 00000
PS3	=> 11011



13,15,17,18,43	+1.0V_VGA		+1.0V_VGA
15,17,18,25,43	+1.8V_VGA		+1.8V_VGA
13,16,17	+3V_DELAY		+3V_DELAY

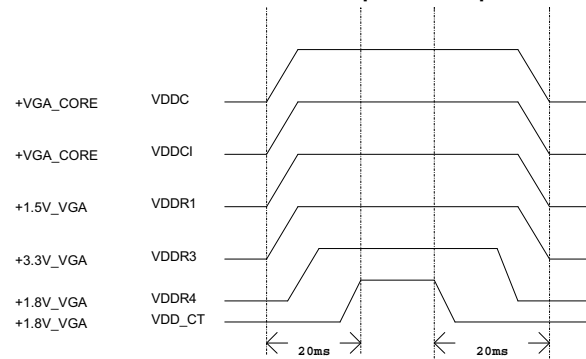






CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512kbit M25P05A (STD) 101 - 1Mbit M25P10A (STD) 101 - 4Mbit M25P40 (STD) 100 - 512kbit Fm25LV512 (Chingis) 101 - 1Mbit Fm25LV010 (Chingis)	001
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYN	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled Reserve for future ASIC	1
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE- ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111

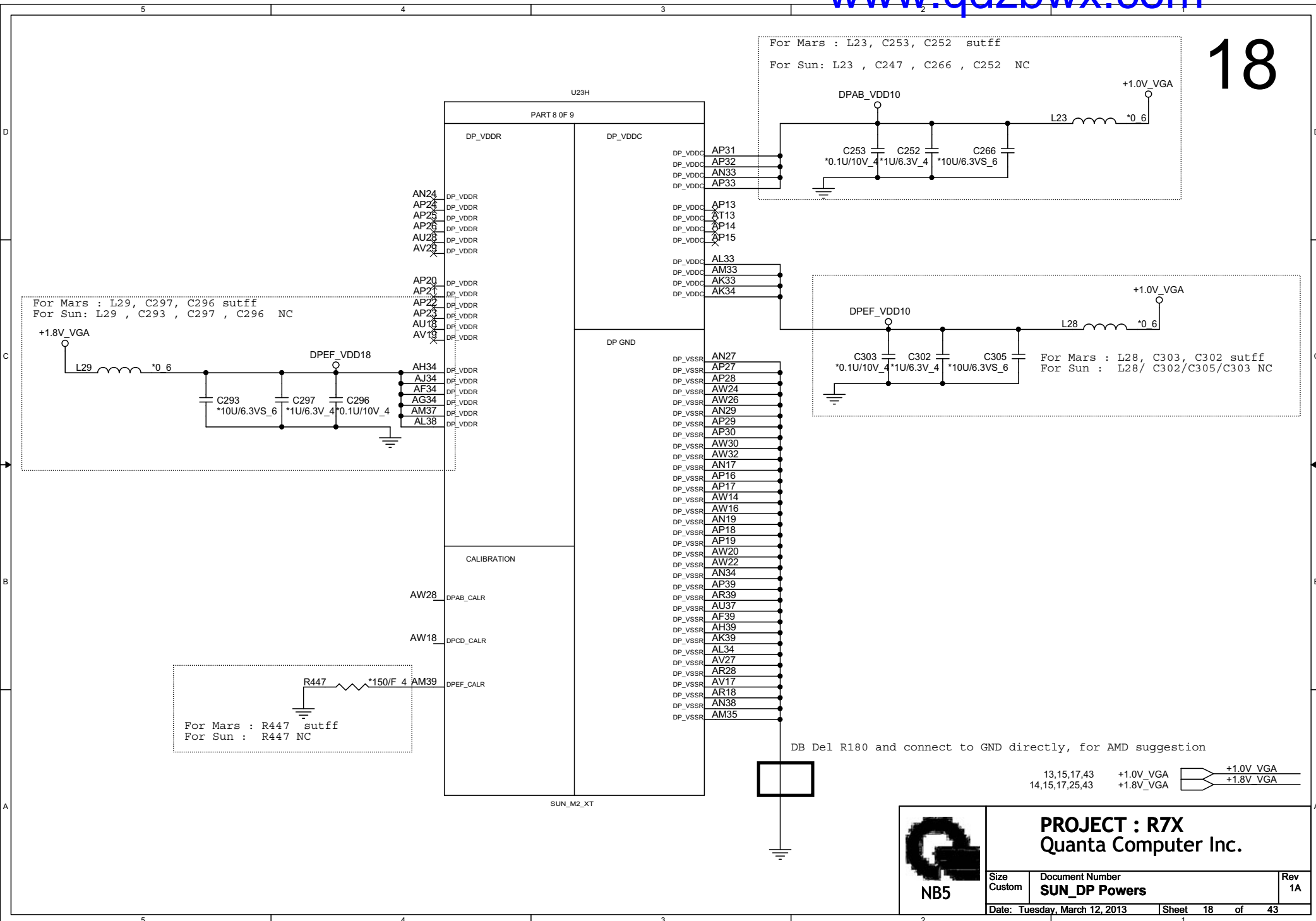
Power Up/Down Sequence



PROJECT : R7X
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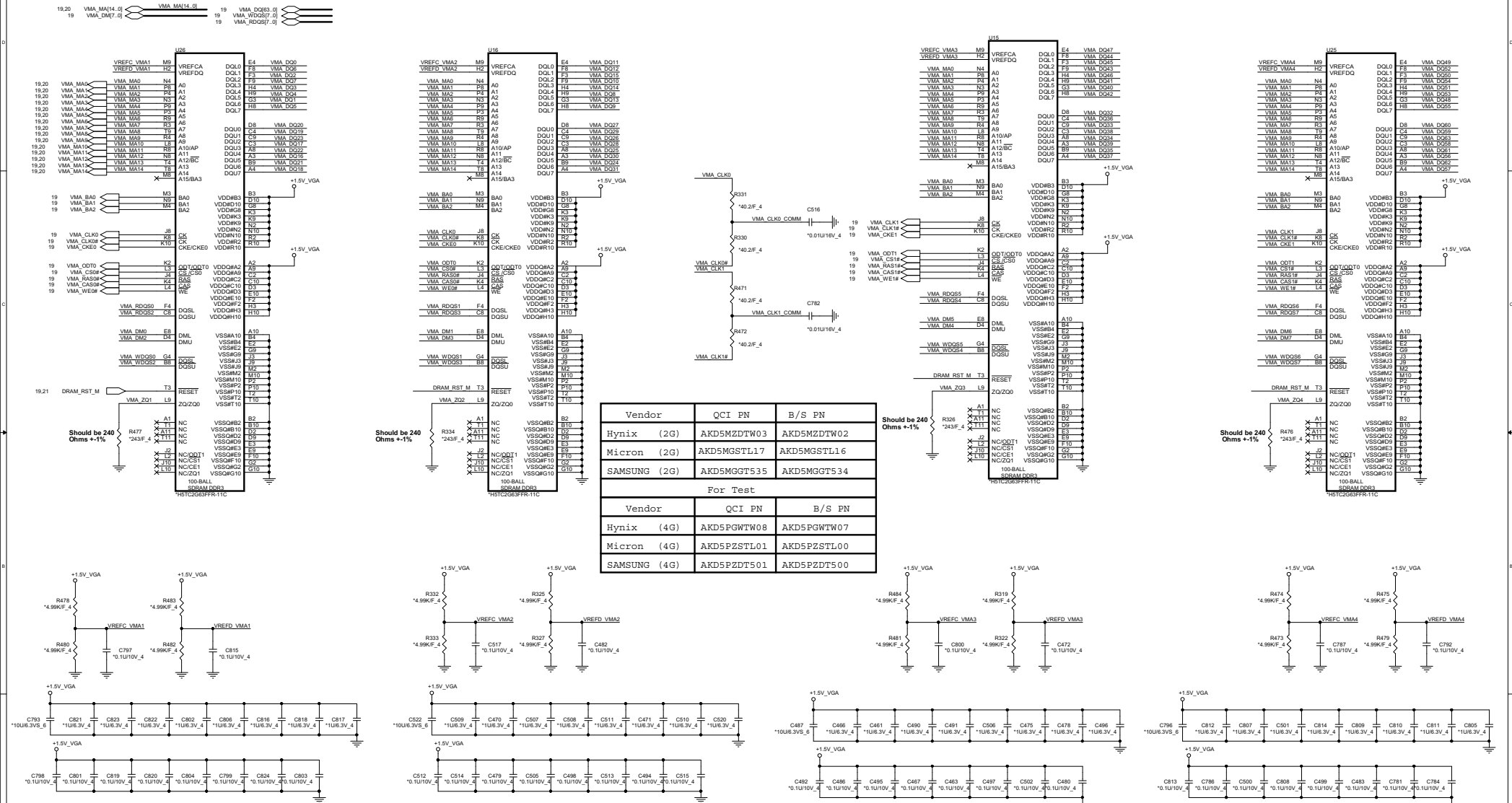
Size Custom Document Number SUN_LVDS / STRAP Rev 1A
Date: Tuesday, March 12, 2013 Sheet 16 of 43



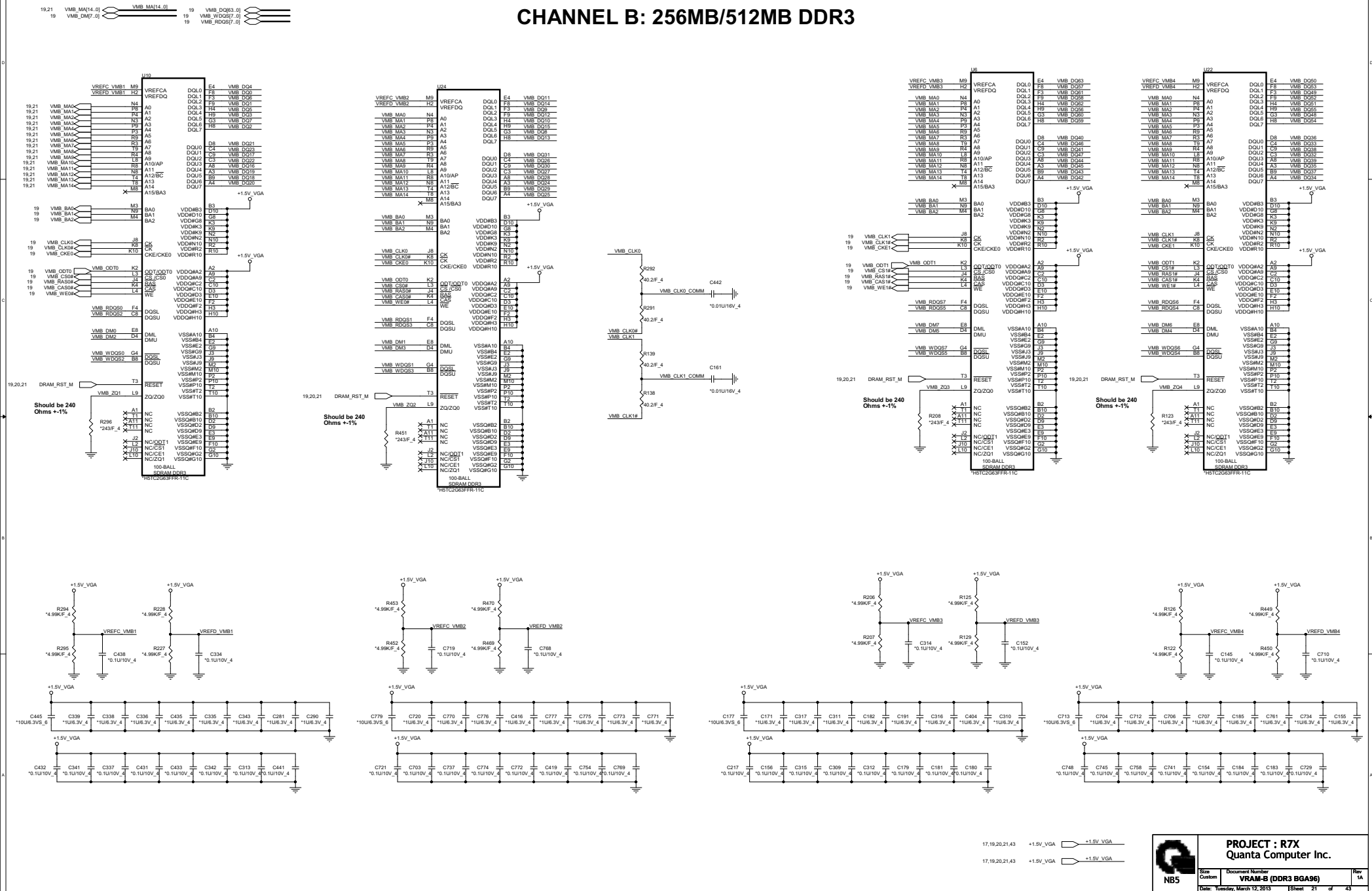




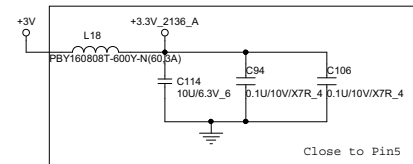
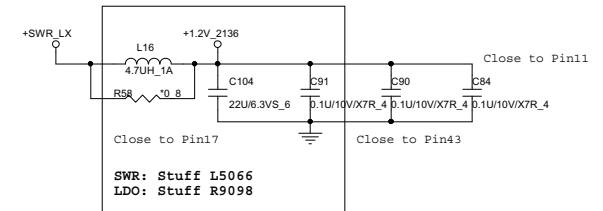
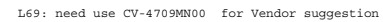
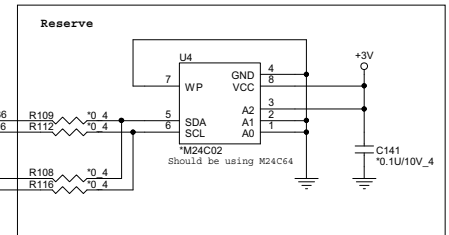
CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

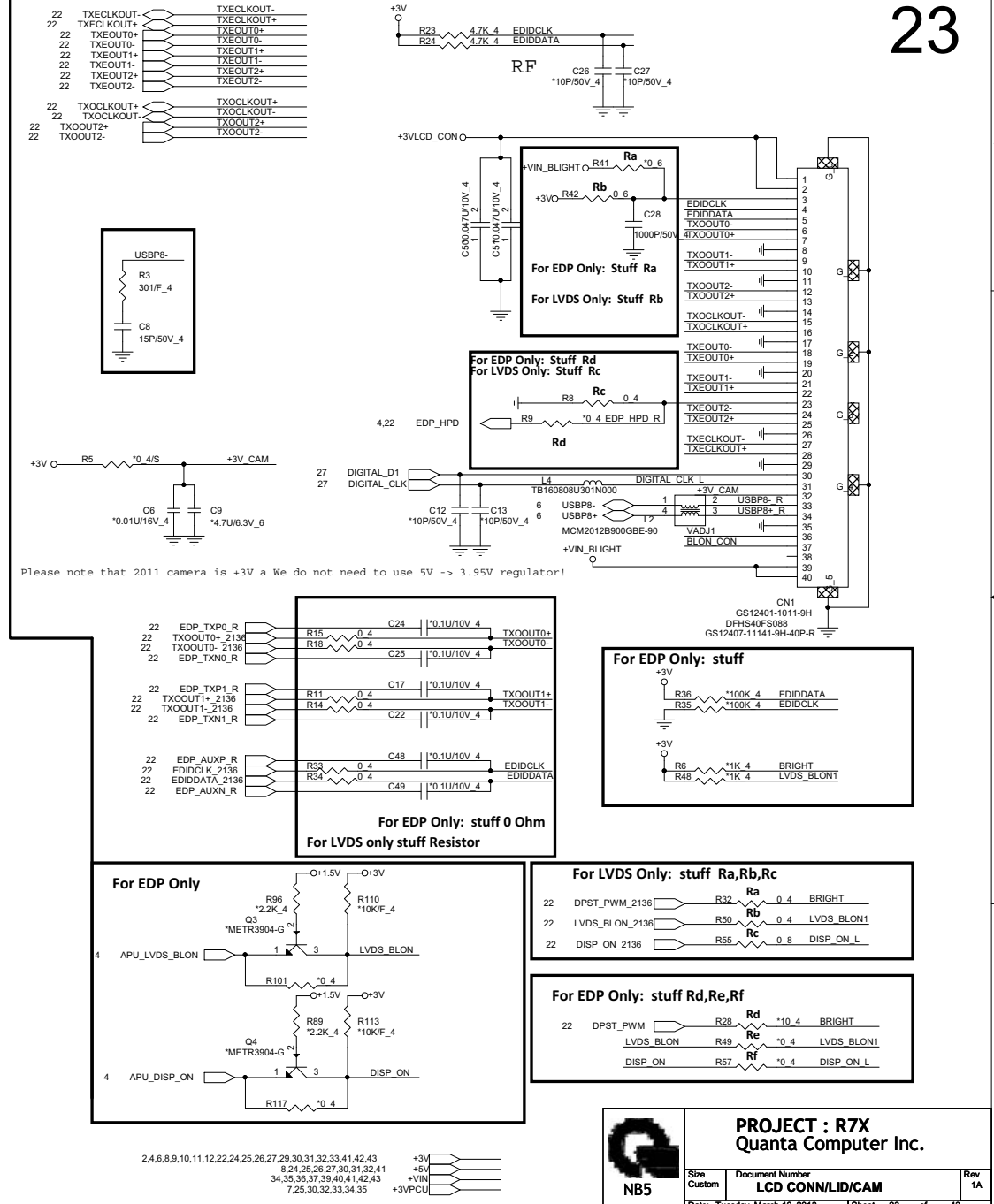
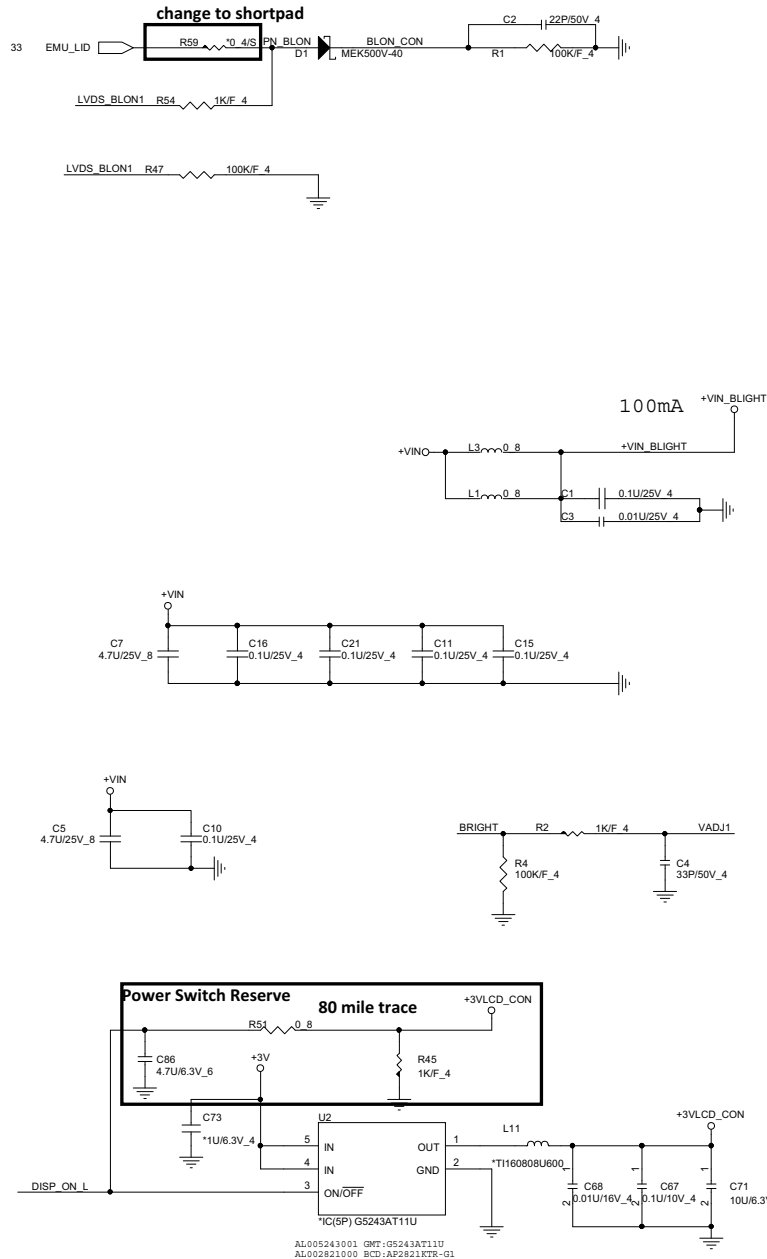


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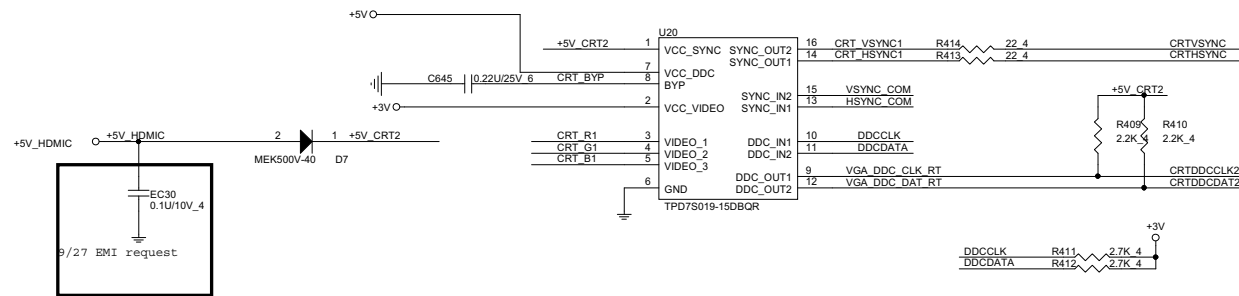
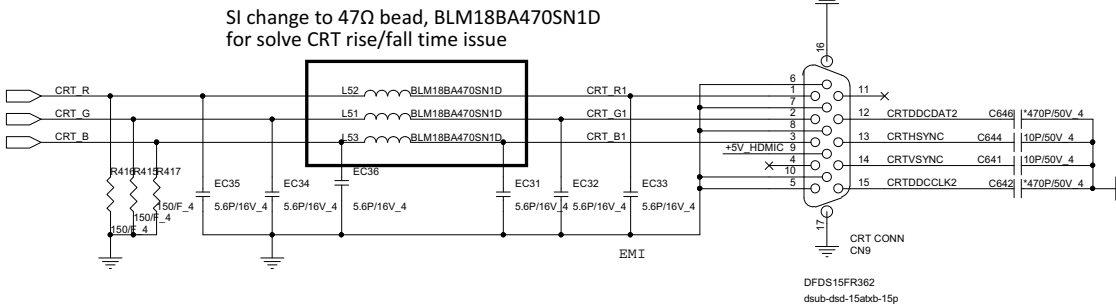
LID Switch



PROJECT : R7X
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Custom	LCD CONN/LID/CAM	1A
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CRT PORT



HOLE

HOLE

FAN hole

PCH BKT

CPU BKT

VGA BKT

Nut PN:MBBU2005010

THERMAL BKT

KB lock

SI add

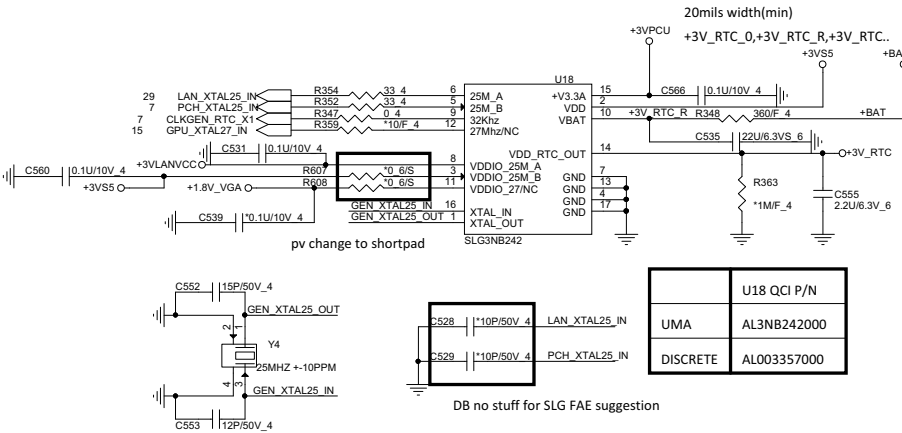
MV add



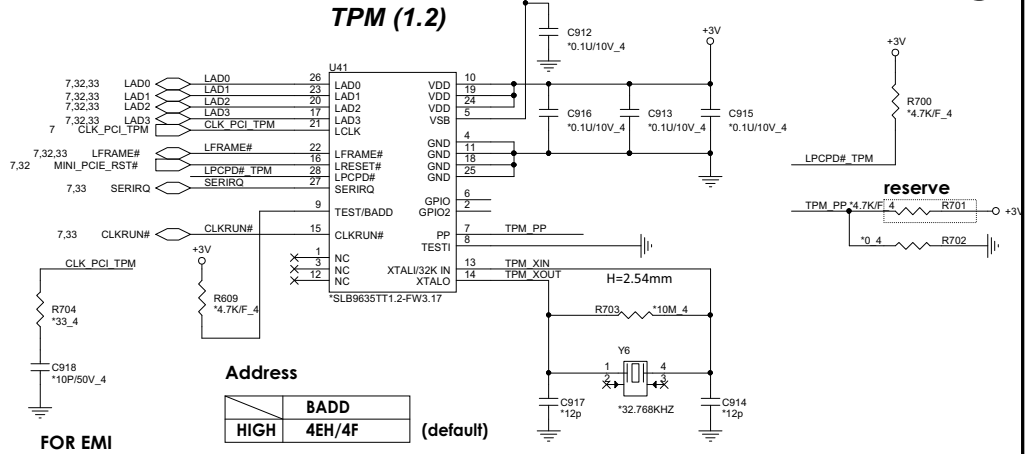
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT_Hole	1A
Date:	Tuesday, March 12, 2013	Sheet 24 of 43

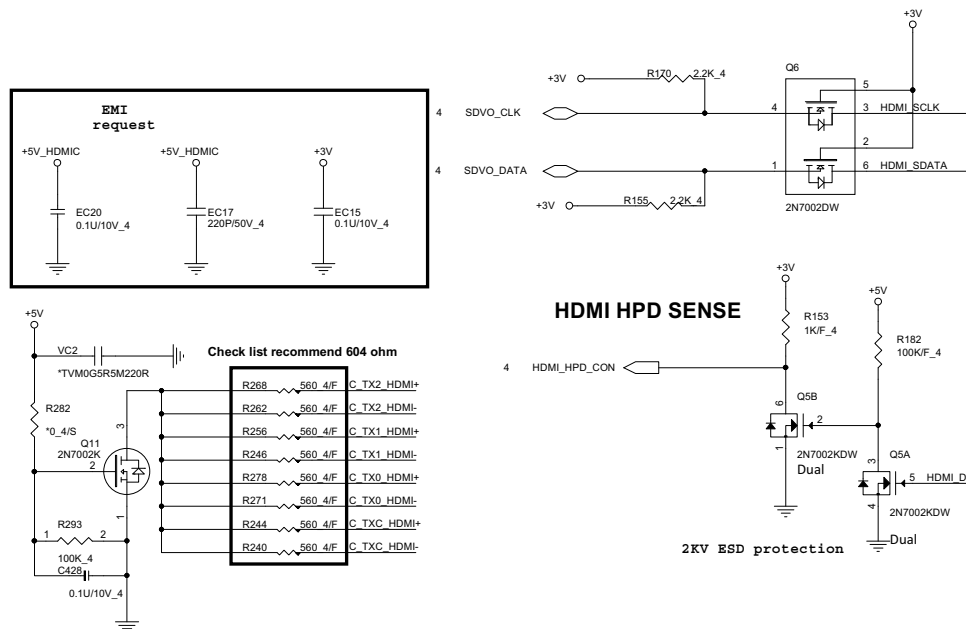
Green CLK Circuitry



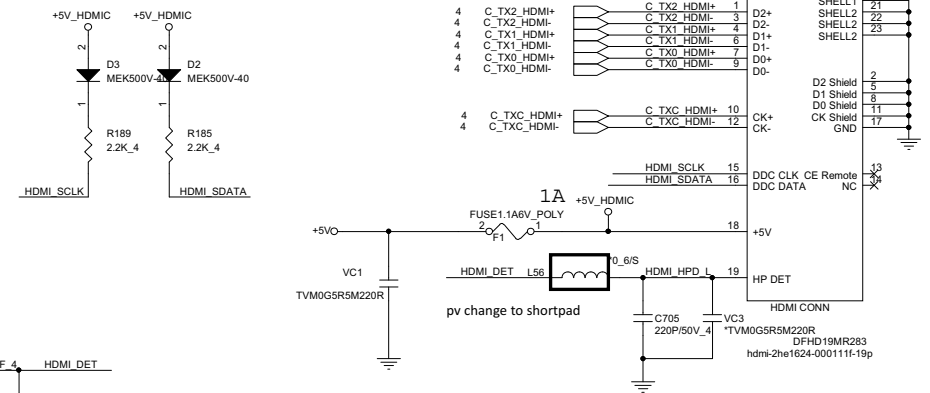
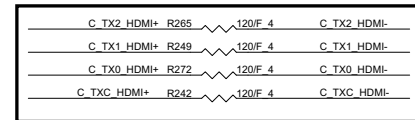
PV add



DISCRETE HDMI I2C SELECT Close to HDMI Connector

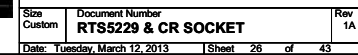


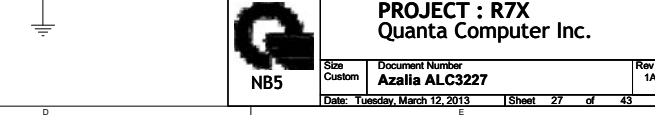
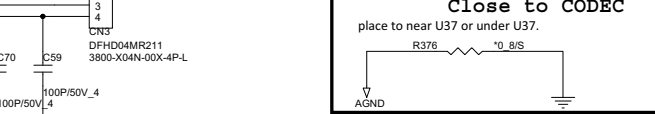
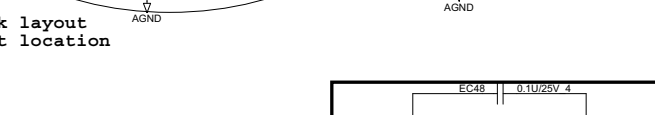
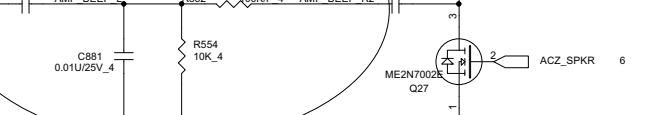
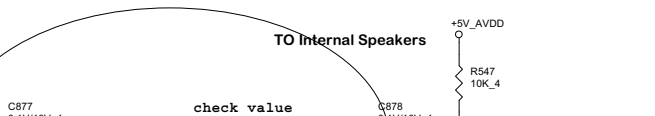
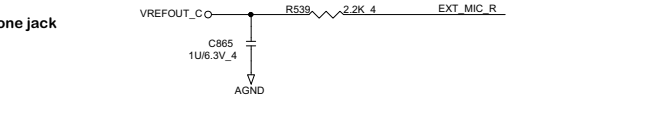
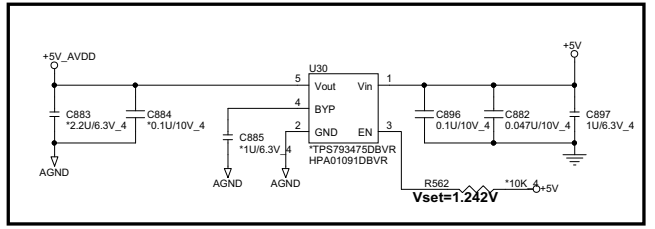
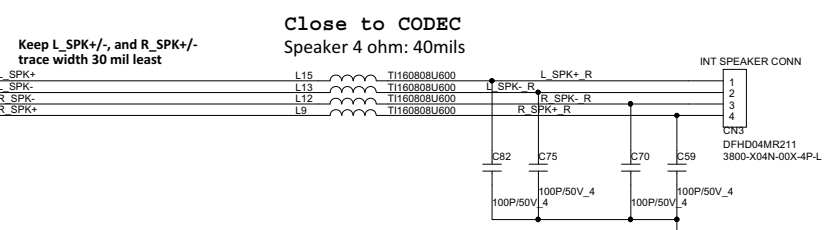
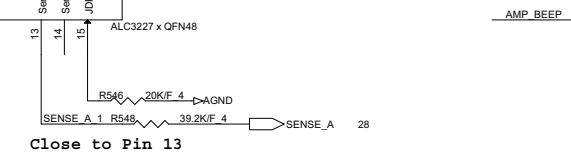
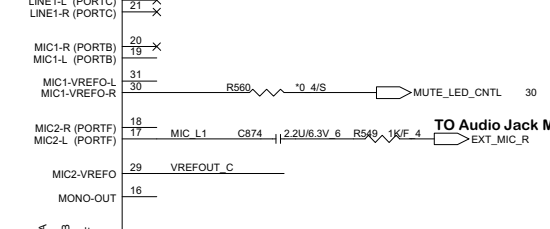
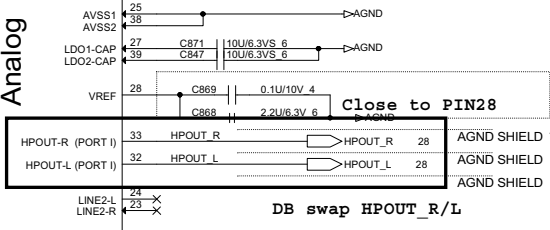
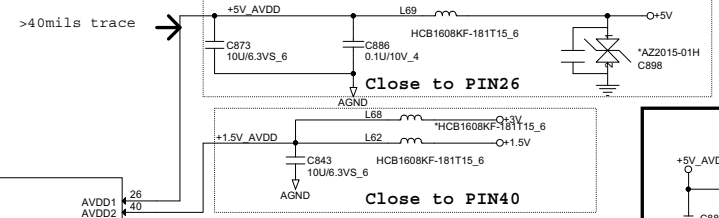
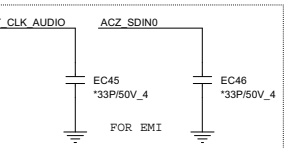
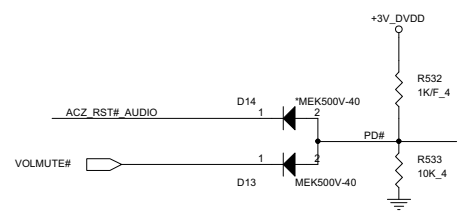
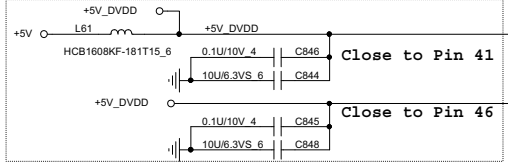
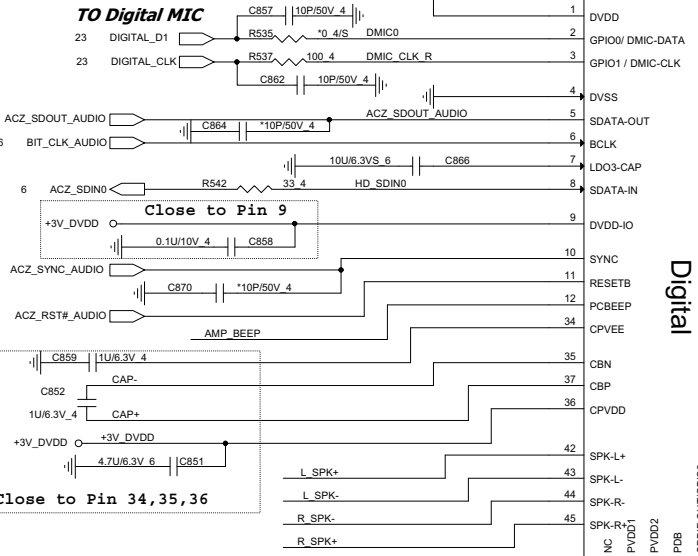
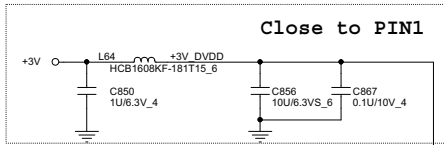
EMI request



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Quanta Computer Inc.

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Custom	HDMI	1A
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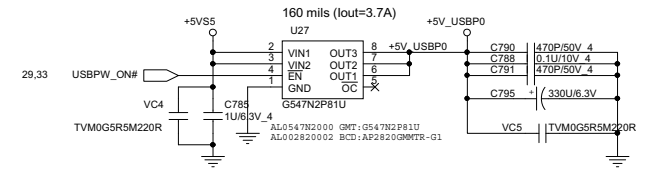
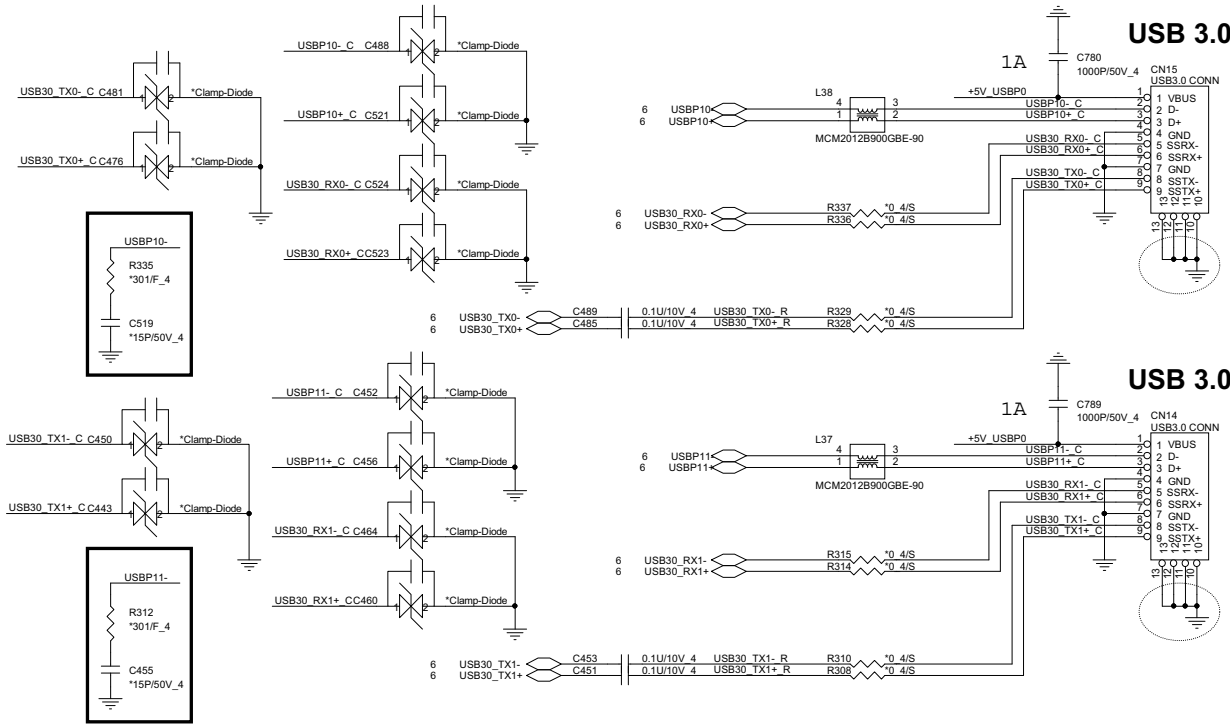




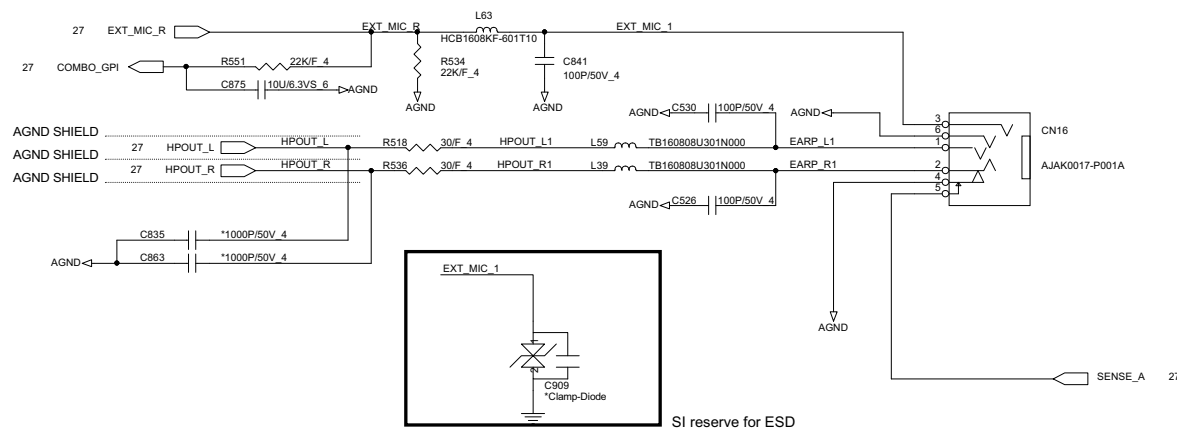
PROJECT : R7X
Quanta Computer Inc.


Size: Custom
 Document Number: Azalia ALC3227
 Date: Tuesday, March 12, 2013
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USB3.0 X 2/USB2.0 COMBO

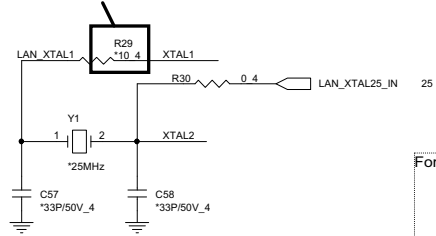


COMBO JACK



	PROJECT : R7X Quanta Computer Inc.	
	Size Custom	Document Number USB/Audio Jack
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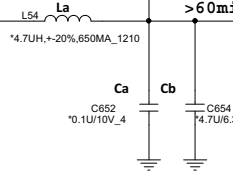
For EMI 0 ~ 22 ohm



Trace < 30 mil
Width > 60 mil

Power trace Layout 宽度 > 60mil

> 60mil

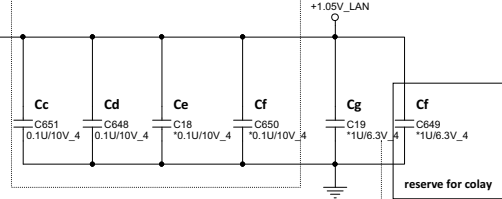


For GbE
Stuff La, Ca, Cb

For 10/100
NA: La, Ca, Cb

For GbE
* Place Cc, Cd, Ce, Cf
close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA Ce, Cf
* Place Cc, Cd
close to each VDD10 pin-- 8, 30 only,



For GbE
* Place Cg close to each VDD10 pin-- (reserve)

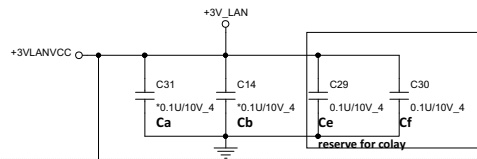
For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

For 10/100

* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA

* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23, 32

For GIGA
Stuff Cc, Cd

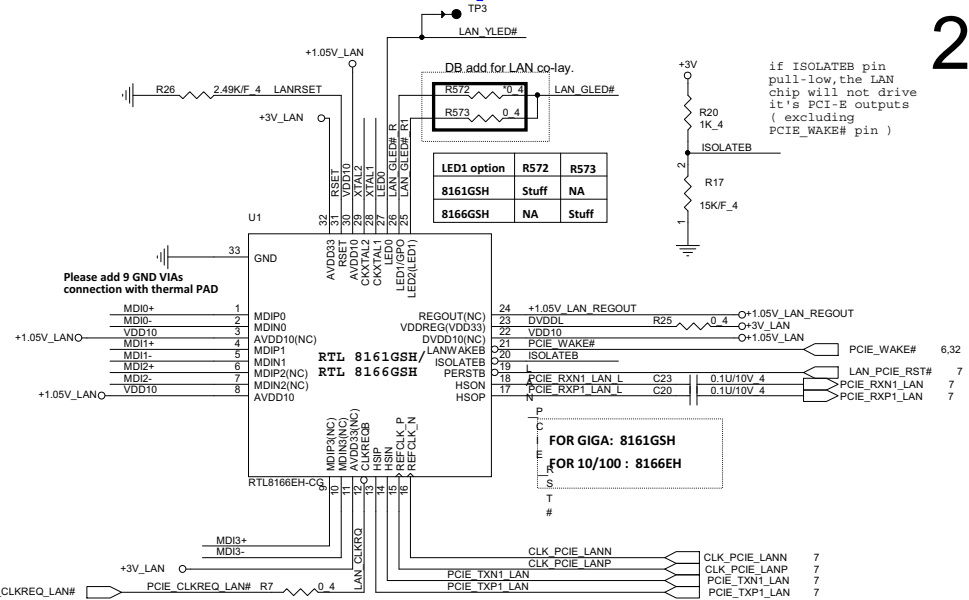
For 10/100

NA: Cc, Cd

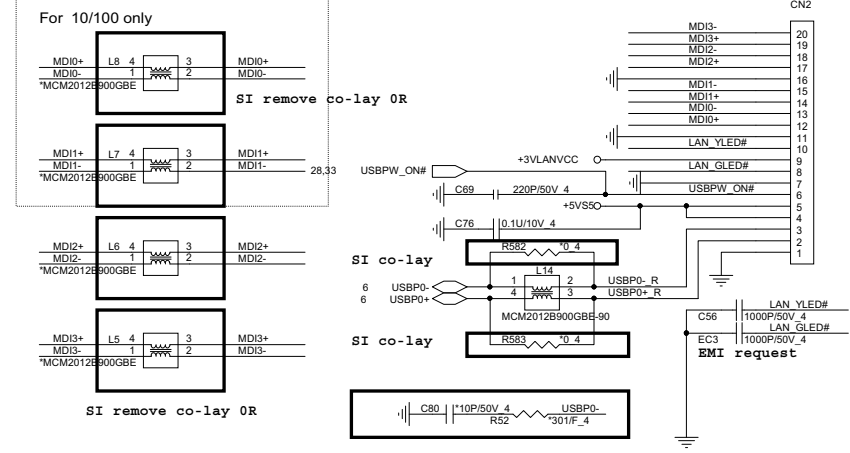
Remove For Not Using SWR mode

2,4,6,8,9,10,11,12,22,23,24,25,26,27,30,31,32,33,41,42,43
25,41

+3V
+3VLANVCC



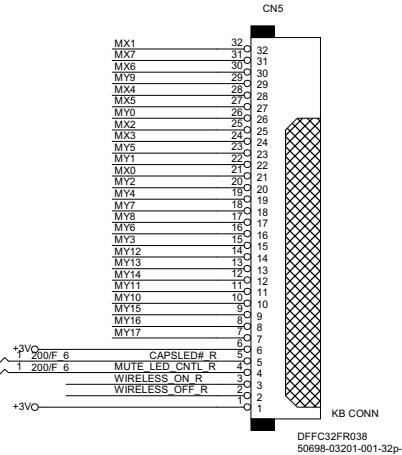
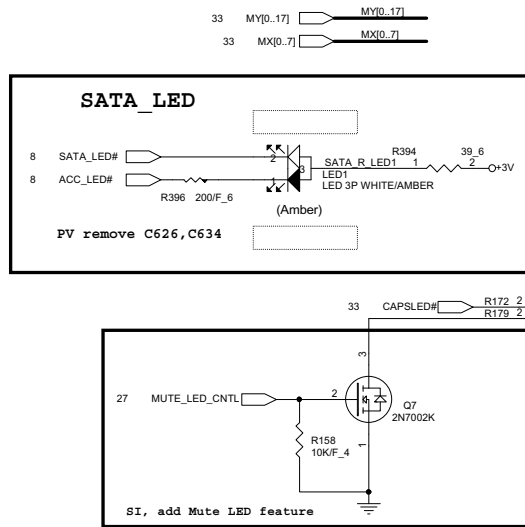
LAN conn & Right SIDE USBX1



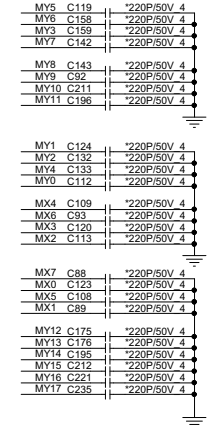
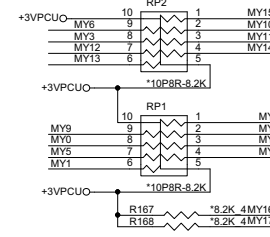
PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number RTL 8105E/RJ45	Rev 1A
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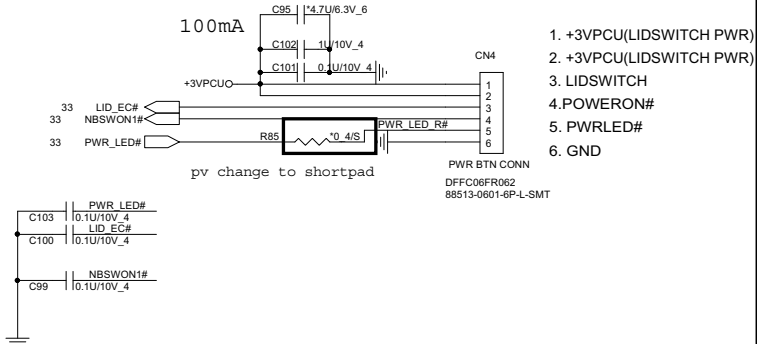
KEYBOARD Con.



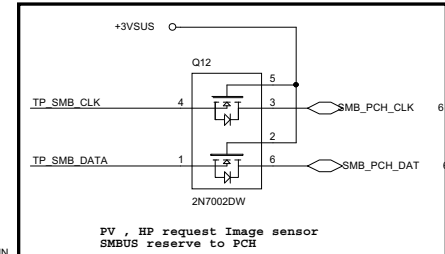
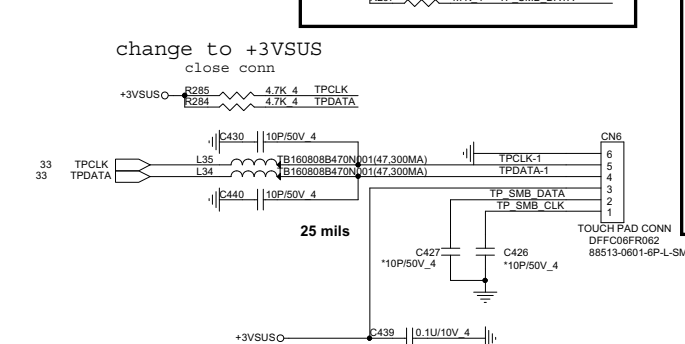
KEYBOARD PULL-UP



POWER BOTTON CONNECT



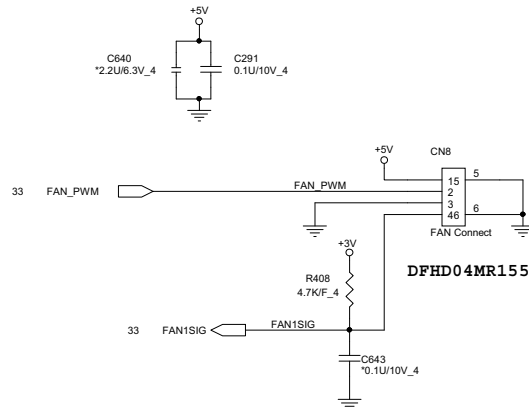
TOUCH PAD Con.



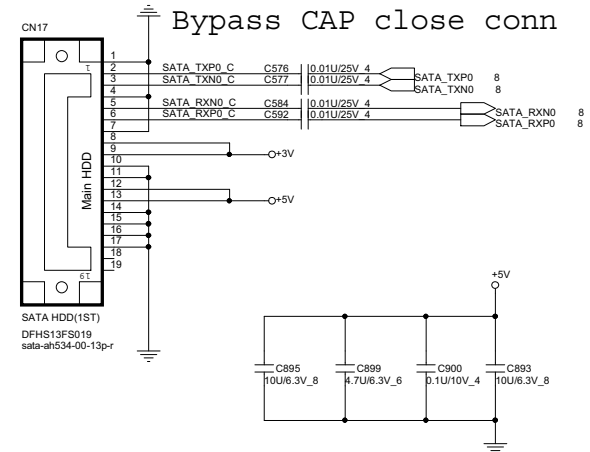
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A
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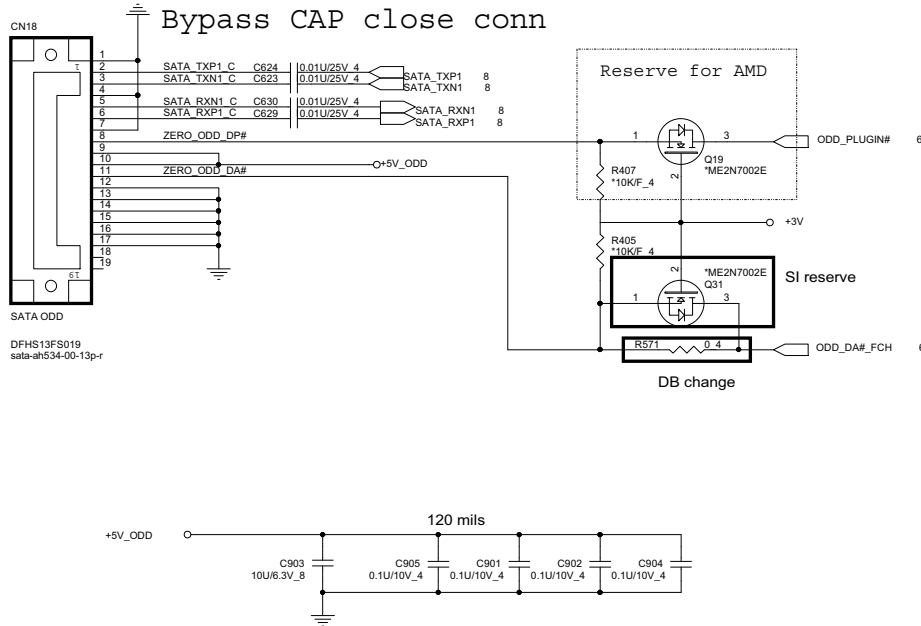
CPU FAN



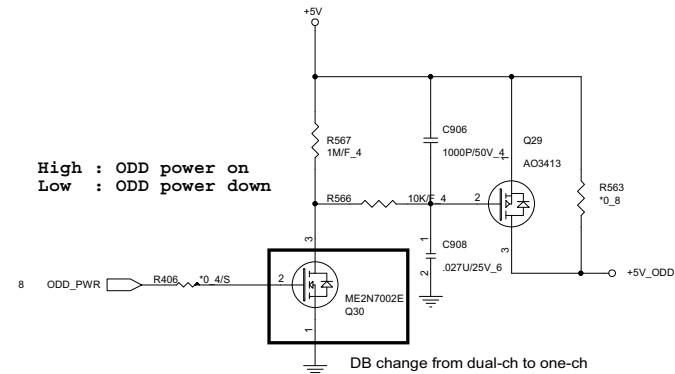
SATA HDD CONNECTOR



SATA ODD CONNECTOR

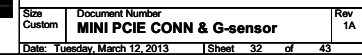


High : ODD power on
Low : ODD power down

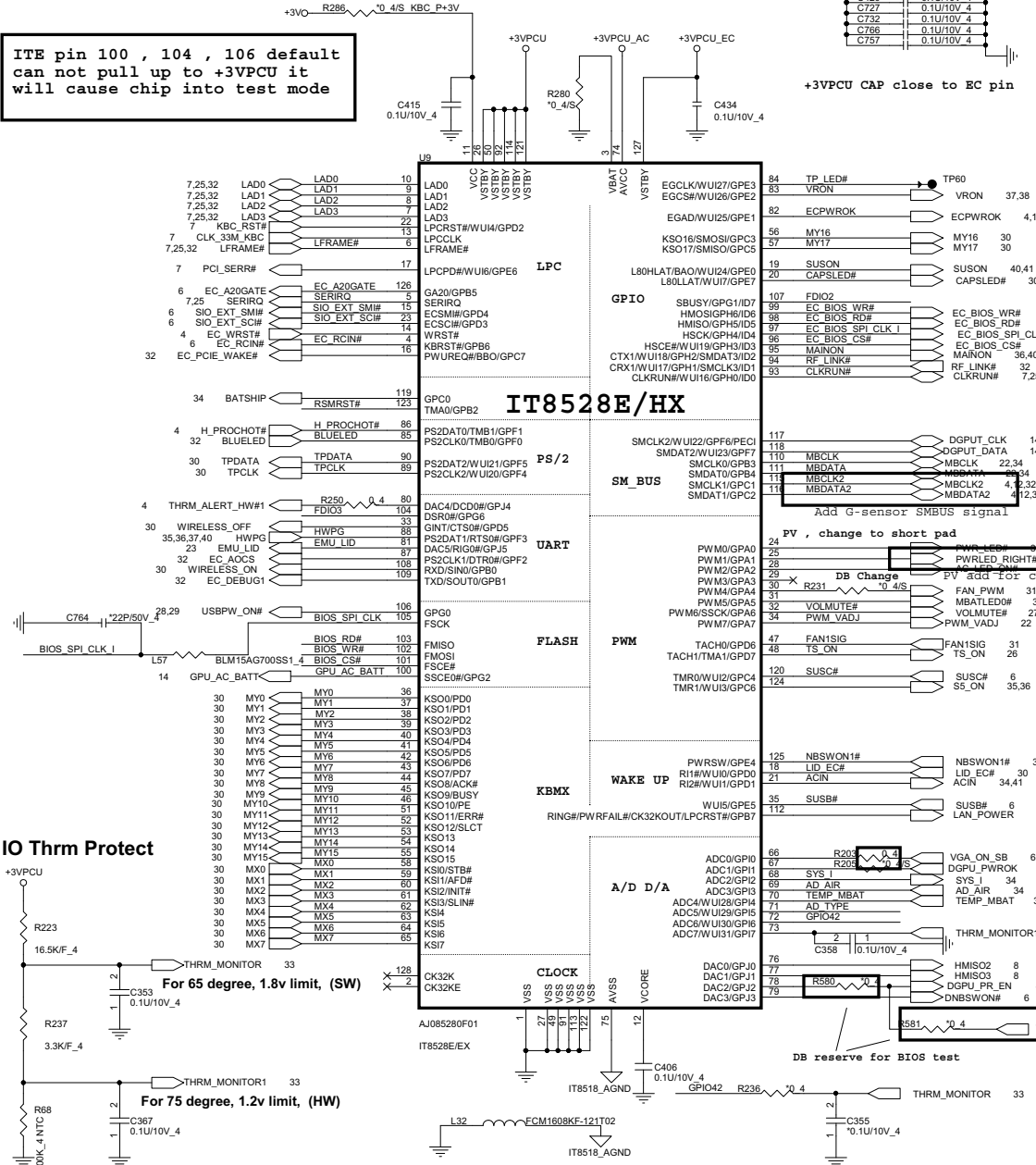


DB change from dual-ch to one-ch

2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,33,41,42,43 +1.5V
7,25,30,33,34,35 +3V
8,24,25,26,27,30,31,41 +3VPCU
+5V

[illegible]

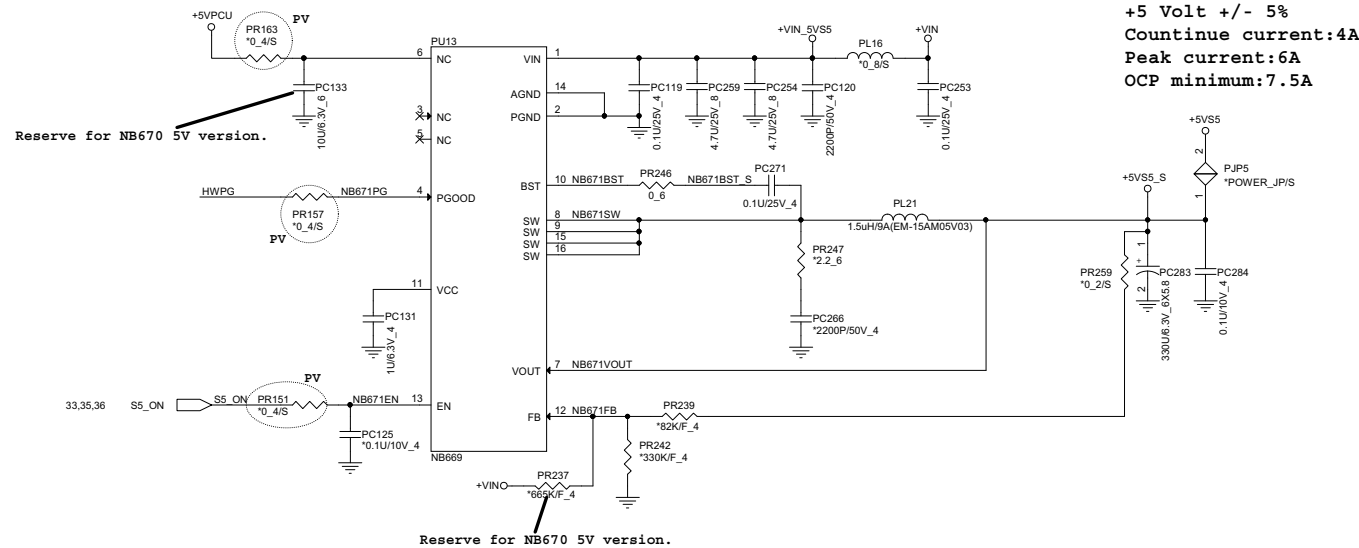
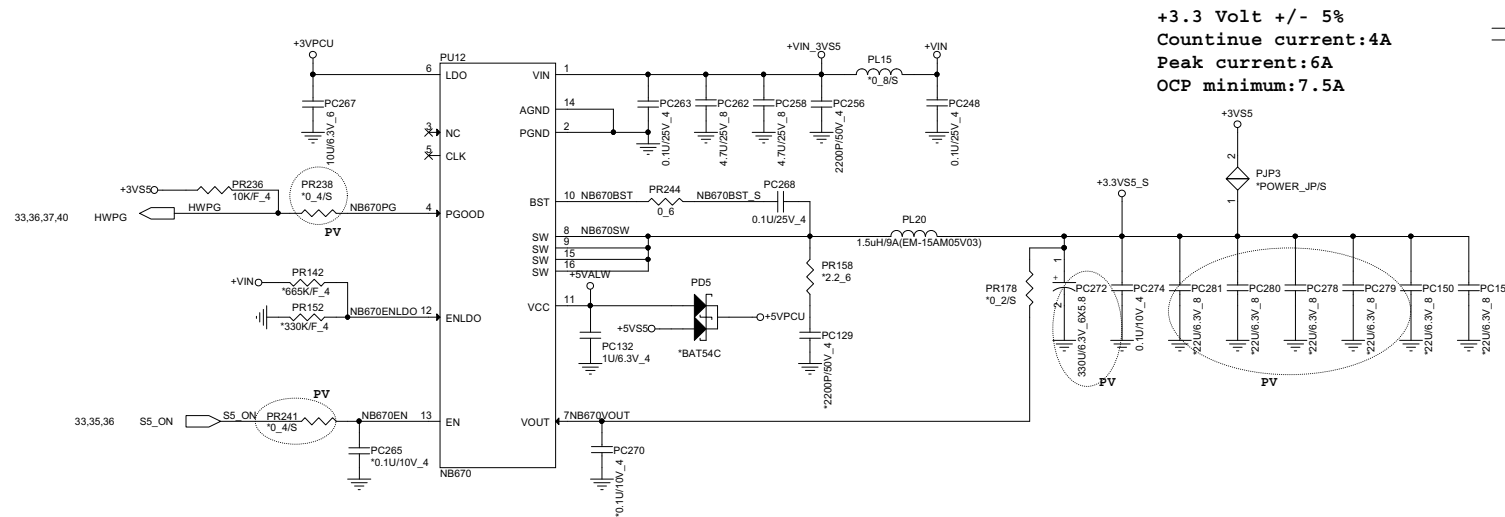
ITE pin 100, 104, 106 default can not pull up to +3VPCU it will cause chip into test mode



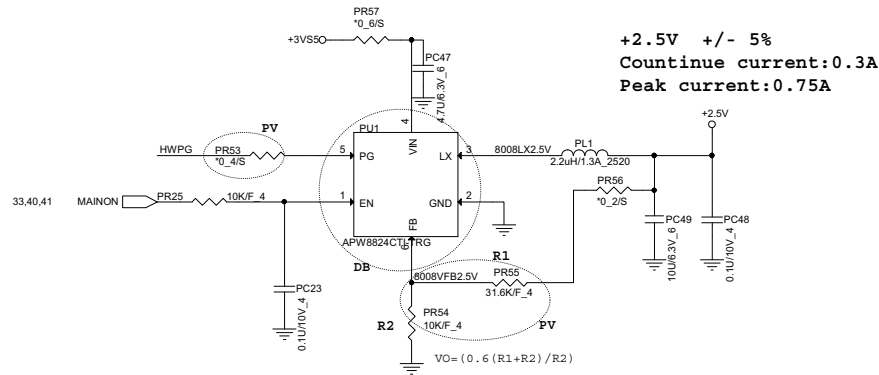
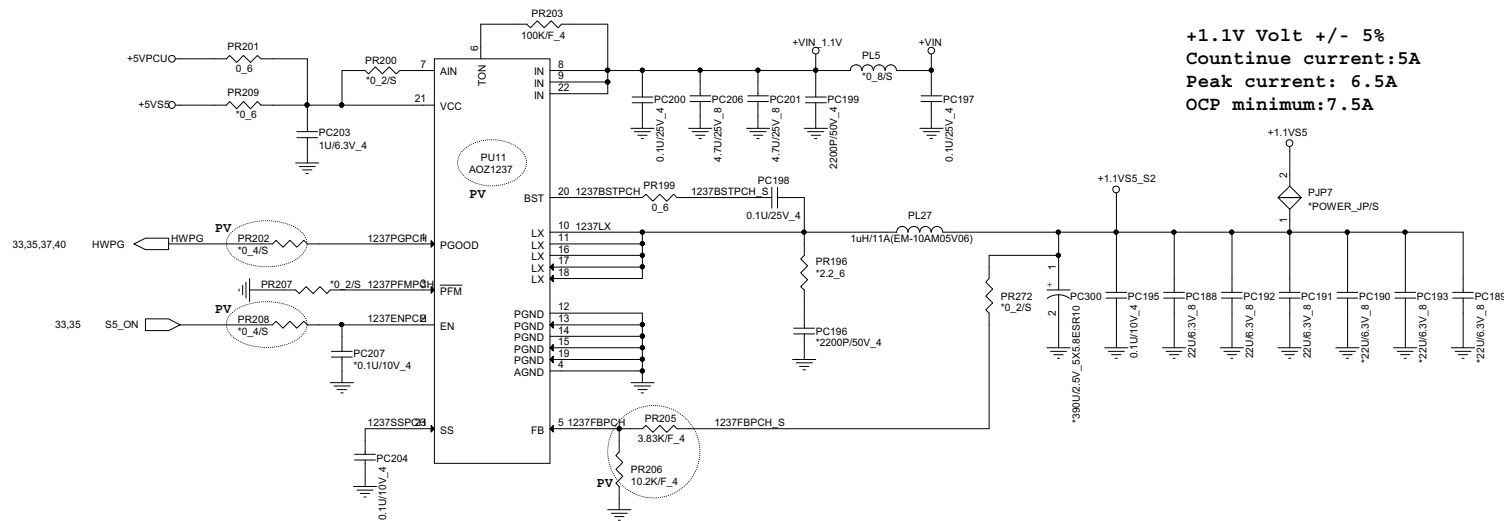


Size Custom	Document Number Charger (BQ24728)	Rev 1A
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DC/DC +3VS5/+5VS5



	PROJECT : R7X		
	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VS5 (NB670/NB671)	Rev 1A
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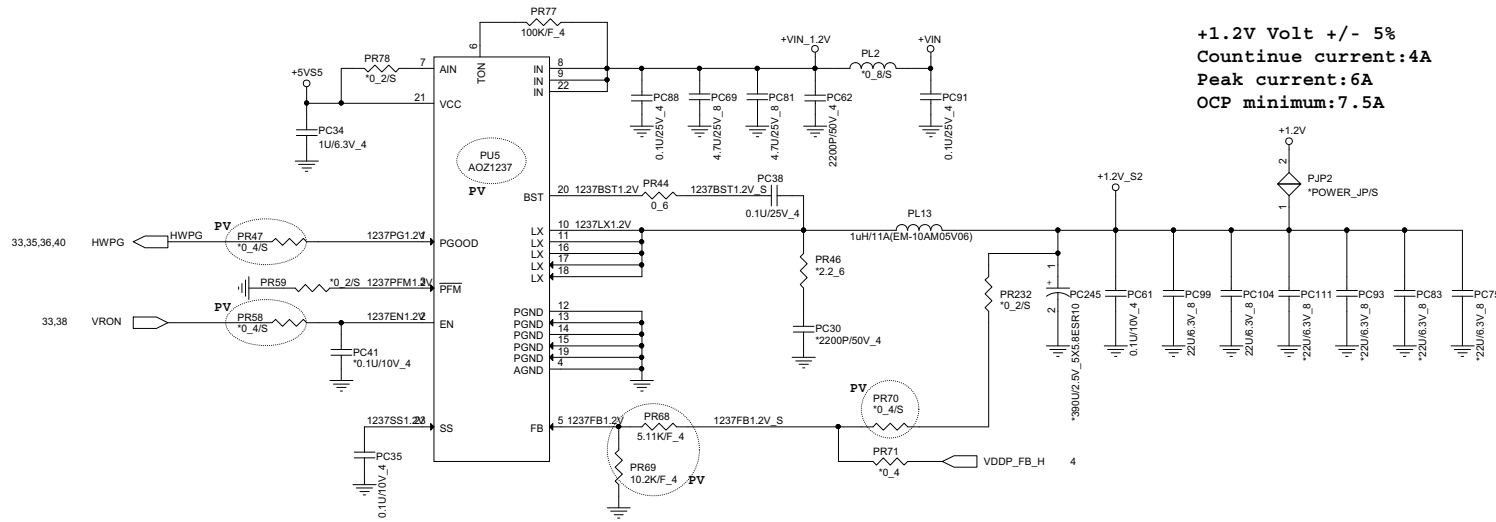


+VIN	23,34,35,37,39,40,41,42,43
+2.5V	5
+3VSS	4,6,8,9,10,25,32,33,35,38,41,43
+5VSS	28,29,35,37,38,39,40,41,42,43
+1.1VSS	9,41
+5VPCU	34,35



PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number +1.1VSS (AOZ1237)/2.5V	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 36 of 43	

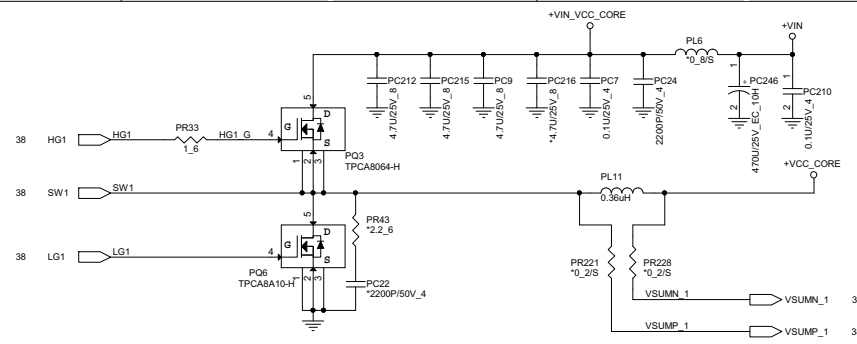


PROJECT : R7X
Quanta Computer Inc.

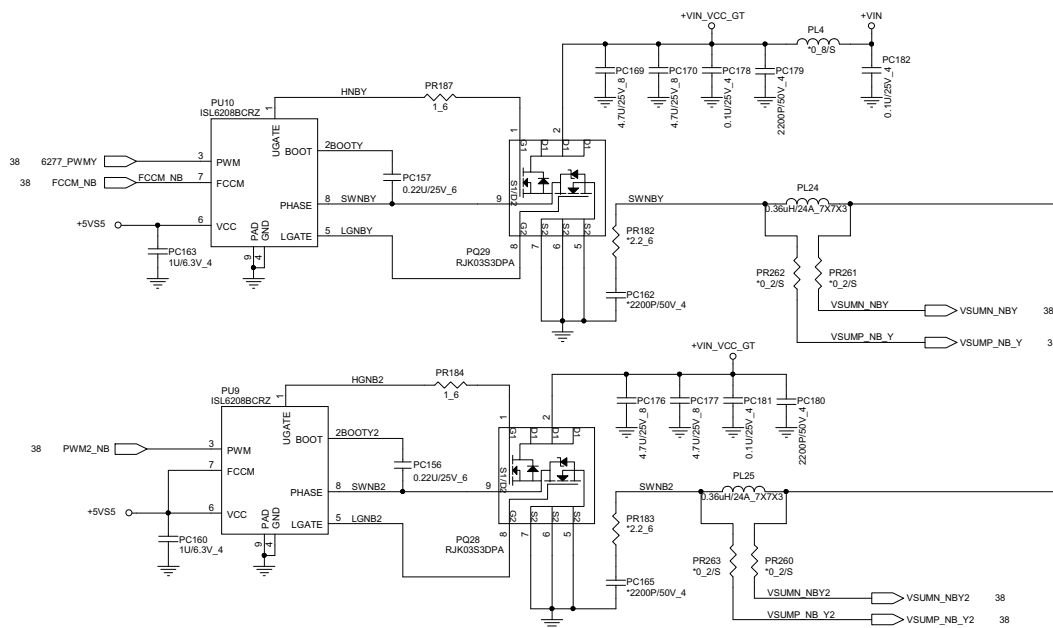
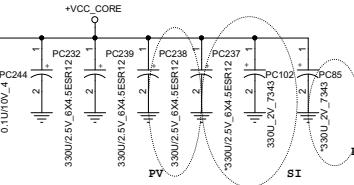
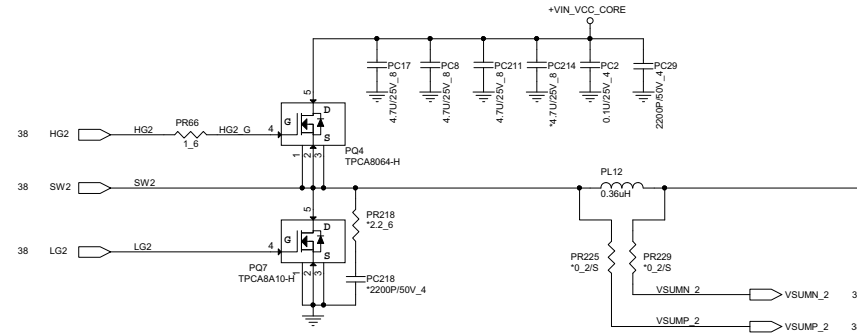
Size	Document Number	Rev
Custom	+1.2V (AOZ1237)	1A
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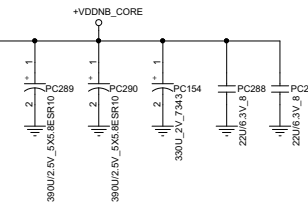
Size Custom	Document Number CPU Core1 (ISL6277)	Rev 1A
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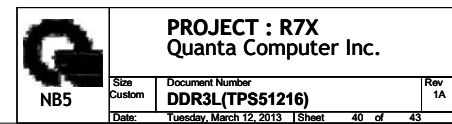
CPU CORE Volt
 Countinue current:36A
 Peak current:50A
 OCP minimum:60A



VDDNB Volt
 Countinue current:25A
 Peak current:33A
 OCP minimum:40A



	PROJECT : R7X Quanta Computer Inc.		
	Size Custom	Document Number CPU Core2 (ISL6208)	Rev 1A
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Size Custom	Document Number Dis-charge IC (SLG55448V)	Rev 1A
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VGA Core

42

+VGA_CORE 17.43

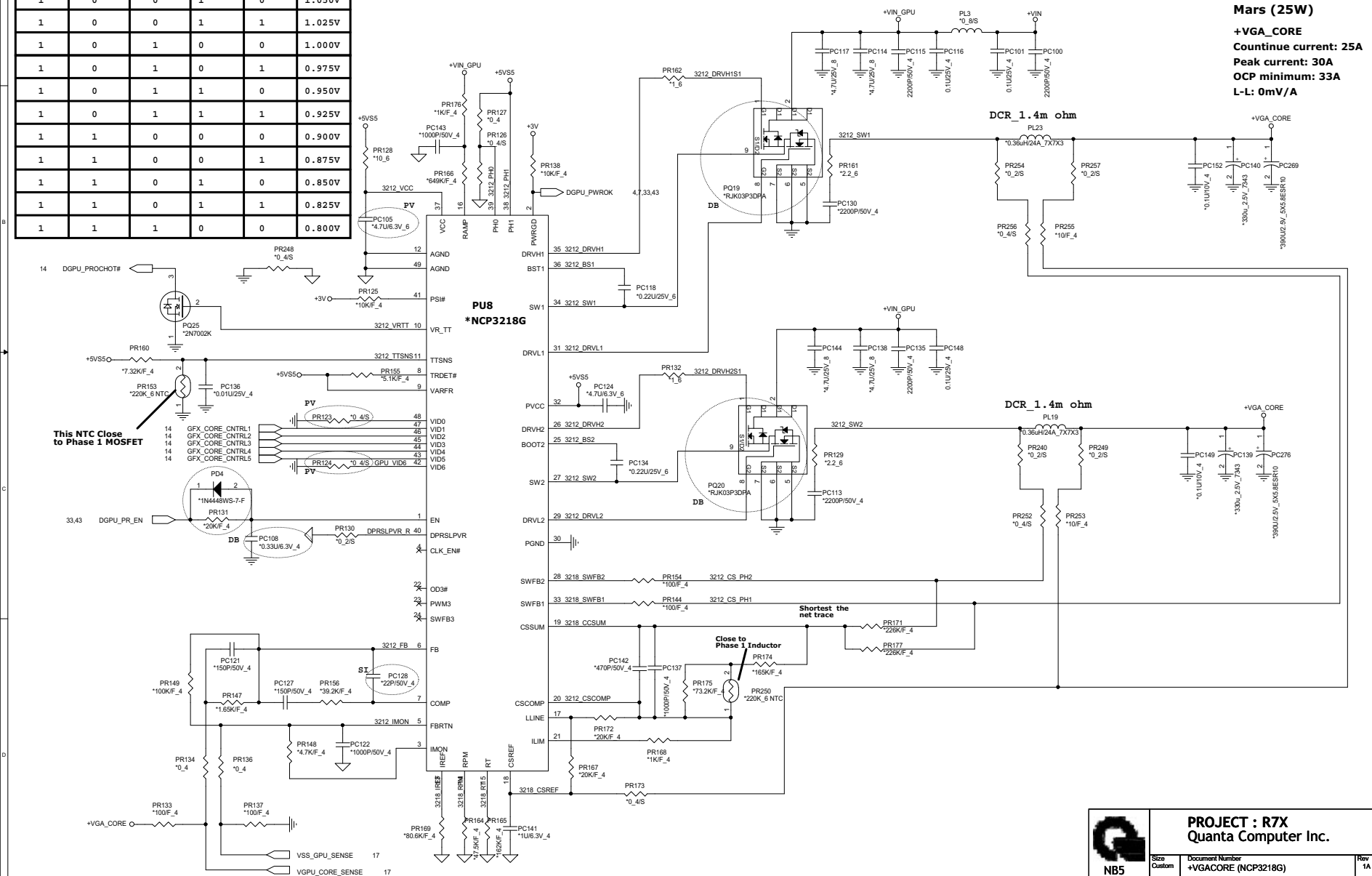
Mars (25W)

+VGA_CORE
Continue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

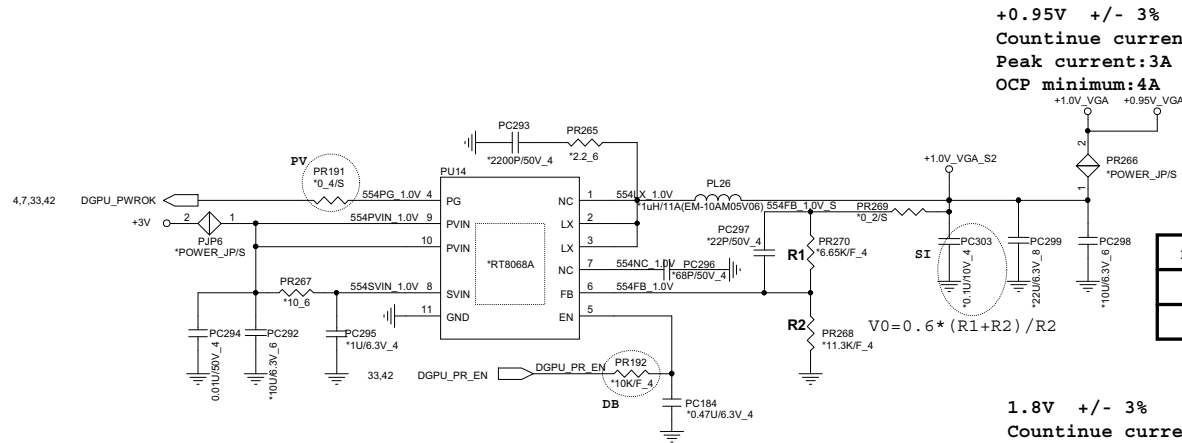
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

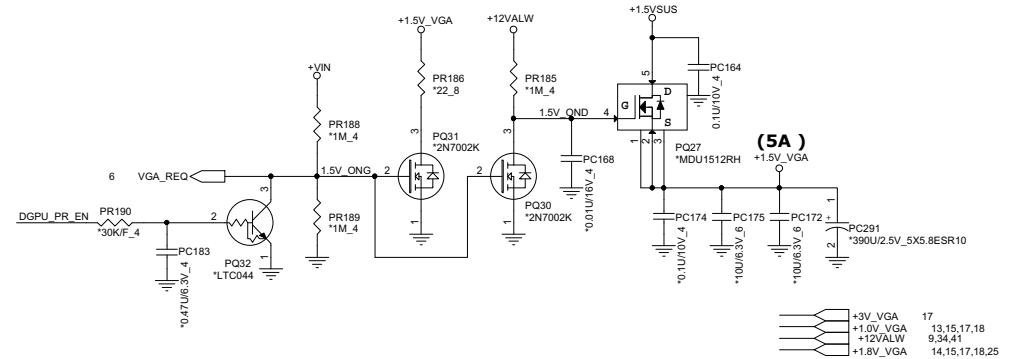
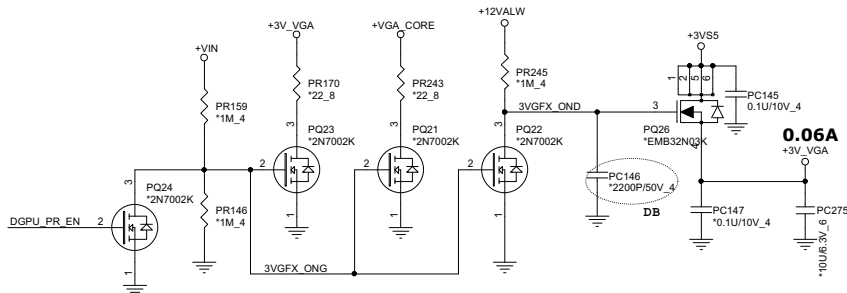
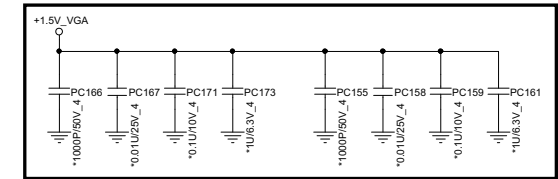
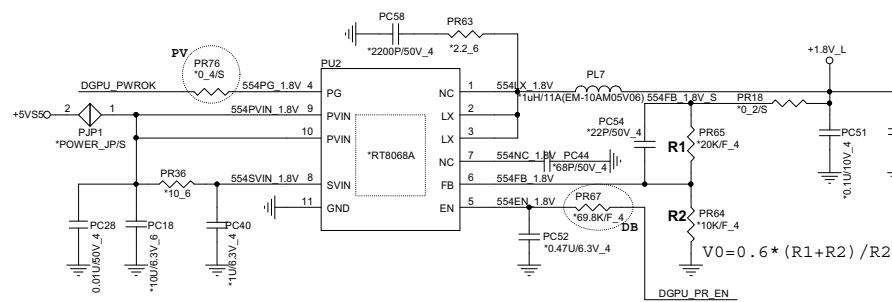


PROJECT : R7X
Quanta Computer Inc.

Size: Custom
Document Number: +VGA CORE (NCP3218G)
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Rev: 1A



R2 Value	P/N	1.0V_VGA
10K	C831002FB26	1.0V
11.3K	C831132FB07	0.95V



+3V_VGA 17
+1.0V_VGA 13,15,17,18
+12V_VGA 9,34,41
+1.8V_VGA 14,15,17,18,25



PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA/1.8V_VGA/3V_VGA	1A
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